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TITLE: Computer faults-errors simulator e.g. for reliability studies - has output of third bus shapers unit connected to digital inputs of memory units

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PATENT-FAMILY:

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SU 1564628 A	May 15, 1990	N/A	000	N/A

APPLICATION-DATA:

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ABSTRACTED-PUB-NO: SU 1564628A

BASIC-ABSTRACT: The computer faults and error simulator includes memory units (17,18), encoder (18), registers (19-22), bus shapers (23-29), address decoder (31), clock pulse generator (32), multiplexer (33), RS flipflops (34-36) and pulse shaper (37). The operation principle is based on distortion of data (address-data) during its transmission over the interfaces in a tested system (computer). The memory (17) is for storage distortion code for each simulated fault.

USE/ADVANTAGE - For experimental studying reliability and stability of redundant structure computing systems contg. different async. interfaces. Wider functional scope. Bul.18/15.5.90.

CHOSEN-DRAWING: Dwg.1/3

TITLE-TERMS:

COMPUTER FAULT ERROR SIMULATE RELIABILITY STUDY OUTPUT THIRD BUS SHAPE UNIT
CONNECT DIGITAL INPUT MEMORY UNIT

DERWENT-CLASS: T01

EPI-CODES: T01-G02; T01-G09;

SECONDARY-ACC-NO:

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